

Curriculum Vitae

Philip H. Sweany

Computer Science and Engineering Department
University of North Texas
Denton, Texas 76203
(940) 369-7427
sweany@cs.unt.edu

EDUCATION:

Doctor of Philosophy in Computer Science.
Colorado State University, Dec, 1992.
Dissertation title: “Inter-Block Code Motion Without Copies”
Master of Science in Computer Science.
Colorado State University, May, 1986.
Bachelor of Science in Computer Science.
Washington State University, May, 1983.

CURRENT RESEARCH INTERESTS:

Efficient memory system design,
Compiler optimization in support of efficient memory system design,
Code Generation for Multi-Core Architectures,
Code Generation for Multithreaded Architectures,
Code Generation for Instruction-Level Parallel Architectures,
Efficient use of scratch-pad memory

CURRENT SOFTWARE PROJECTS:

Rocket Compiler
Hy-C Compiler

WORK IN PROGRESS:

Design and evaluation of compiler techniques to generate efficient code on multi- and many-core computers,
Investigation of tools to design, compile, and execute programs on hybrid multi-core architectures, i.e., those containing FPGAs, and/or ASICs, as well as general purpose CPUs,
Experimental evaluation of the level of thread parallelism that can be exploited in imperative programs,

REFEREED JOURNAL PUBLICATIONS:

- Huang, J., Li, H., and Sweany, P., FPGA Implementations of Elliptic Curve Cryptography and Tate Pairing over a Binary Field, *Journal of Systems Architecture*, V. 54, No.12, December 2008, pp. 1077-1088.
- Li W., Rezaei M., Kavi K., Naz A., and Sweany P., Feasibility of Decoupling Memory Management From the Execution Pipeline, *Journal of Systems Architecture: the EURO-MICRO Journal*, V. 53, No. 12, 2007, pp. 927-936.
- Naz A., Kavi, K., Sweany, P., and Li W., Tiny Split Data Caches Make Big Performance Impact for Embedded Applications, (Special Issue: Embedded Single-Chip Multicore Architectures and Related Research - from System Design to Application Support), *Journal of Embedded Computing*, Vol. 2, No. 2, 2006, 207-219.
- Naz A., Rezaei, M., Kavi, K., and Sweany, P., Improving Data Cache Performance With Integrated Use Of Split Caches, Victim Cache And Stream Buffers, *March 2005 special issue of ACM SigArch Computer Architecture NEWS – Best Papers of MEDEA-2004*, pp 41-48.
- Carr, S., and Sweany, P., An Experimental Evaluation of Scalar Replacement on Scientific Benchmarks, *Software Practice and Experience*, Vol. 33, No.15, December 2003, pp 1419-1445.
- Bedy, M.J., Carr, S., Onder, S. and Sweany, P., Improving Software Pipelining by Hiding Memory Latency with Combined Loads and Prefetches, in *Interaction between Compilers and Computer Architectures*, G. Lee and P.-C. Yew ed., Kluwer Academic Publishers, 2001 pp. 69-88.
- Allan V., Beaty S., Su B., and Sweany P., Building a Retargetable Local Instruction Scheduler, *Software Practice and Experience*, volume 28:3, pages 249-84, March 1998, pp. 249-283.
- Sweany P., Huber, B.L., and Carr S., Global Instruction Scheduling Without Copies, *Digital Technical Journal* 10(1), December 1998, pp. 58-70.
- Mueller, R.A., Duda, M.R., Sweany, P.H. and Walicki, J.S., Horizon: A Retargetable Compiler for Horizontal Microarchitectures, *IEEE Transactions on Software Engineering*, volume 14, number 5, May 1988, pp. 575-583.

BOOK CHAPTERS:

- Williamson, W. J., and Sweany, P. Revitalizing Discipline-Specific Instruction in Technical Communication, in *Innovative Approaches to Technical Communication*, Tracy Bridgeford Karla Kitalong, and Dickie Selfe, (Ed.), Utah State Press, 2004. pages 60-80.

REFEREED CONFERENCE PUBLICATIONS:

- Burke, P., and Sweany P., Automatic Code Generation Through Model-Driven Design, *20th Systems and Software Technology Conference (SSTC 2008)*, Las Vegas NV, April 2008.
- Huang, J., Li, H., and Sweany, P., An FPGA Implementation of Elliptic Curve Cryptography for Future Secure Web Transactions, *Proceedings of the 20th International Conference on Parallel and Distributed Computing Systems (PDCS-2007)*, Las Vegas NV, September 24-26, 2007, pp 296-301.

- Li, W., Kavi, K., Naz, A., and Sweany, P., Speculative Thread Execution in a Multi-threaded Dataflow Architecture, *Proceedings of the ISCA 19th International Conference on Parallel and Distributed Computing (PDCS-2006)*, San Francisco, California, September 20-22, 2006.
- Naz, A., Kavi, K., Sweany P., and Li, W., A Study of Reconfigurable Split Data Caches and Instruction Caches, *Proceedings of the ISCA 19th International Conference on Parallel and Distributed Computing (PDCS-2006)*, San Francisco, California, September 20-22, 2006.
- Naz, A., Kavi, K., Sweany, P., and Li, W., Improving Data Cache Performance with Integrated Use of Split Caches, Victim Cache And Stream Buffers, *Proceedings of the Workshop on Memory performance Dealing with Applications, Systems and Architecture (MEDEA-2004)*, held in conjunction with Parallel Architectures and Compiler Technology Conference (PACT-2004), Sept. 29-Oct. 3, 2004, Antibes Juan-Les-Pins, France.
- Carr, S., and Sweany, P., Automatic Data Partitioning for the Agere Payload Plus Network Processor, *Proceedings of the 8th International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES 2004)*, September 22-25, 2004 pps. 238-247.
- Naz, A., Kavi, K., Sweany, P. and Rezaei, M., A Study of Separate Array and Scalar Caches *Proceedings of the 18th International Symposium on High Performance Computing Systems and Applications (HPCS 2004)*, Winnipeg, Manitoba, Canada, May 16-19, 2004, pp 157-164.
- Sweany P., and Carr, S., Building a C Compiler Retargetable for DSP Processors, *Proceedings of the ODES Workshop*, San Francisco CA, March 2003.
- Qian, Y., Carr, S., and Sweany, P., Optimizing Loop Performance for Clustered VLIW Architectures, *Proceedings of the Eleventh IEEE International Conference on Parallel Architectures and Compiler Techniques (PACT 2002)* 271-280.
- Qian, Y., Carr, S., and Sweany, P., Loop Fusion for Clustered VLIW Architectures, *SIGPLAN 2002 Workshop on Languages, Compiler, and Tools for Embedded Systems (LCTES 2002)*, pp. 112-119.
- Sule, D., Carr, S., and Sweany, P., Evaluating Register Bank Partitioning with Genetic Algorithms, *Conference on Massively Parallel Computing Systems, 2002 (MPCS 2002)*.
- Huang, X., Carr, S., and Sweany, P., Loop Transformations for Architectures with Partitioned Register Banks, *SIGPLAN 2001 Workshop on Languages, Compiler, and Tools for Embedded Systems (LCTES 2001)*, pp. 48-55.
- Hiser, J., Carr, S., Sweany, P., Global Register Partitioning, *International Conference on Parallel Architectures and Compilation Techniques (PACT 2000)* pp 13-23.
- Hiser, J., Carr, S., Sweany, P., and Beaty S.J., Register Assignment for Software Pipelining with Partitioned Register Banks *International Parallel and Distributed Processing Symposium (IPDPS 2000)*, 211-217.
- Williamson, W.J., and Sweany P., Linking Communication and Software Design Courses for Professional Development in Computer Science, *In Language and Learning Across the Disciplines*, 1999.
- Sweany P., and Beaty S., Instruction Scheduling Using Simulated Annealing, *Conference on Massively Parallel Computing Systems (MPCS '98)*.

- Kuras, D., Carr S., and Sweany P., Value Cloning for Architectures with Partitioned Register Banks, In *The 1998 Workshop on Compiler Support for Embedded Systems (CASES98)*.
- Jang S., Carr S., Sweany P., and Kuras D., A Code Generation Framework for VLIW Architectures with Partitioned Register Files, *Conference on Massively Parallel Computing Systems (MPCS '98)*,
- Ding C.H., Carr S., and Sweany P.H., Modulo Scheduling with Cache Reuse Information, Euro-Par'97 Workshop on Instruction-Level Parallelism. In *Euro-Par'97 Parallel Processing, Proceedings of the Third International Euro-Par Conference*, August 1997, pp 1079-1083.
- Cho P., George D., Ott L., Predebon W., and Sweany P. New Faculty Orientation and Seminar Series: Emphasis on Teaching and Learning, *Proceedings of 1996 ASEE Annual Conference*, June 1996.
- Beaty S.J., Colcord S., and Sweany P.H., Using Genetic Algorithms to Fine-Tune Instruction Scheduling, *Proceedings of the Second International Conference on Massively Parallel Computing Systems*, Ischia, Italy, May 1996.
- Carr S., Ding C.H., and Sweany P.H., Improving Software Pipelining with Unroll-and-Jam, *Proceedings of the 29th Annual Hawaii International Conference on System Sciences*, Maui, Hawaii, Jan, 1996, pp 183-192.
- Bourke M., Sweany P.H., and Beaty S. Extending List Scheduling to Consider Execution Frequency, *Proceedings of the 29th Annual Hawaii International Conference on System Sciences*, Maui, Hawaii, Jan, 1996, 193-202.
- Brasier T.S., Sweany P.H., Carr S., and Beaty S.J., CRAIG: A Practical Framework for Combining Instruction and Register Assignment, *Parallel Architectures and Compilation Techniques Conference (PACT95)*, Limassol, Cyprus, June, 1995, pp. 11-18.
- Sweany P.H., and Beaty S.J., Dominator-Path Scheduling: A Global Scheduling Method, *Proceedings of the 25th Microprogramming Workshop (MICRO-25)*, Portland, OR, December, 1992, pp. 260-263.
- Sweany P.H., Dominator-Path Scheduling: Inter-Block Code Motion Without Copies, *Ph.D Dissertation, Colorado State University, Ft Collins CO.*, December, 1992.
- Sweany P.H., and Beaty S.J., Post-Compaction Register Assignment in a Retargetable Compiler, *Proceedings of the 23rd Microprogramming Workshop (MICRO-23)*, Orlando, FL, November, 1990, pp. 107-116.
- Howland M.A., Mueller R.A., and Sweany, P.H., Trace Scheduling Optimization in a Retargetable Microcode Compiler, *Proceedings of the 20rd Microprogramming Workshop (MICRO-20)*, Colorado Springs, CO, December, 1987, pp. 106-114.

FUNDED GRANTS:

- *Global Instruction Scheduling Without Copies*, Principal Investigator, National Science Foundation, \$97,649, 1993-96.
- *Research for Undergraduates Supplement to Global Instruction Scheduling Without Copies*, Principal Investigator, National Science Foundation, \$5,000, 1994-95.
- *Research for Undergraduates Supplement to Global Instruction Scheduling Without Copies*, Principal Investigator, National Science Foundation, \$5,000, 1995.

- *Research for Undergraduates Supplement to Global Instruction Scheduling Without Copies*, Principal Investigator, National Science Foundation, \$5,000, 1996.
- *Hiding the Latency Between Level-1 and Level-2 Cache on the DEC Alpha 21164*, Co-Principal Investigator with Steve Carr, Digital Equipment Corporation, \$83,500, 1995-96.
- *Generating Efficient Code for Horizontal Micro- Architectures With Partitioned Register Files*, Co-Principal Investigator with Steve Carr, Texas Instruments, \$23,715, 1995-96.
- *Hiding the Latency Between Level-1 and Level-2 Cache on the DEC Alpha 21164*, Co-Principal Investigator with Steve Carr, Digital Equipment Corporation, \$45,647, 1996-97.
- *Register-Bank Assignment for Distributed-Register, Instruction-Level Parallel Architectures*, Co-Principal Investigator with Steve Carr, Texas Instruments, \$42,830, 1997-98.
- *Building a Retargetable Java Bytecode Compiler*, Michigan Research Excellence Fund Grant, \$30,900, 1997-1998.
- *Code Generation Compiler ILP Architectures with Partitioned Register Banks*, Principal Investigator, National Science Foundation, \$325,534, 1998-2001.
- *Substituting CISC Instructions in Compiled DSP Code*, PI, UNT 2004 Research Opportunity Program, \$4,000.
- *Equipping a DSP Lab*, co-PI, TI DSP University Program, submitted December 12, 2003 Equipment worth \$60,000 donated.
- *Recruiting and Retention Strategies for Computer Science at UNT*, co-PI, Texas Technology Workforce Development Grant Program, \$125,322.
- *Proposed Conference Support for SCOPES 05*, PI, National Science Foundation, \$12,500.
- *IUCRC-Planning Proposal: UNT Research Site Proposal to join Embedded Systems I/UCRC*, co-PI, National Science Foundation, \$10,000, September 2007.
- *UNTeach*, Senior Investigator, The National Mathematics and Science Initiative and UTeach Institute, \$2,400,000.
- *Collaborative Research: IUCRC Center Proposal: Net-Centric Software and Systems*, NSF (co-PI) \$349,482 over five years.
- *Retargetable Code Generation for Heterogeneous Multi-Processor Computers*, \$30,000, Texas Instruments, as part of NSF/IUCRC Center (PI)

PENDING GRANTS:

- *Addressing Computational Needs of Multimedia and Medical Applications*, USA Scientific Coordinator (co-PI) , Executive Programme Italy-United States of America, 180,000 Euros over three years.

TEACHING EXPERIENCE:

Tenure Track Associate Professor, 9/2003 – present University of North Texas Computer Science and Engineering Department, Denton, TX. Courses taught (and teaching) include Data Structures(3400), Introduction to Compilers (3650), Special Topics in Compiler Optimization (5890), Automata Theory (5200) Computer Science III (2050), u Operating Sytems (4600), Graduate Operating Systems (5640), Programming Languages (4430), Graduate Programming Languages (5450), Compiler Optimization (5650) and Systems Programming (3600), Research Topics in Compilers (6650).

Adjunct Faculty member, 9/2002 – 5/2003 University of North Texas Computer Science Department. Courses taught (and teaching) include beginning computer architecture (3100) and compilers (5550).

Tenured Associate Professor, 6/98 – 8/2000,

Tenure-track Assistant Professor, 9/92 – 5/98, Michigan Technological University Computer Science Department, Houghton, MI. Courses taught include Introductory Computer Programming, Data Structures, Discrete Mathematics, Software Development Methods, Computers and Society, Systems Software Project, Design and Analysis of Algorithms, Object-Oriented Programming, Compiler Construction, Advanced Compiler Optimization, and Instruction-Level Parallelism.

Instructor, Michigan Technological University Computer Science Department, Houghton, MI. 9/91 – 5/92. Courses taught include Data Structures and Compiler Construction.

Lecturer, Colorado State University Computer Science Department, Fort Collins, CO. 8/90 – 5/91. Courses taught include introductory FORTRAN classes, FORTRAN and C classes for intermediate programmers, and introductory Data Structures.

Lecturer, National Technological University, Fort Collins, CO. 7/90 – 8/90. Co-taught a 52-hour program titled “Comprehensive Unix” through the National Technological University.

Lecturer, Colorado State University Computer Science Department, Fort Collins, CO. 8/84 – 12/85. Courses taught include introductory and intermediate Personal Computing classes, and Comparative Programming Languages.

INDUSTRIAL COMPUTING EXPERIENCE:

Technical Staff, DSP Solutions R&D Center, Texas Instruments, Dallas, TX. 9/00 – 8/03
Member of group that is writing, and supporting, compiler tools for TI’s family of DSPs.

Senior Software Engineer, Quantitative Technology Corporation Fort Collins, CO. 9/87 – 7/89. Part of a team which wrote a production-quality retargetable microcode C compiler. Was involved in all aspects of the production including the detailed algorithm and implementation design, the generation and documentation of C++ code, the testing of resultant product and the maintenance and improvement of the product. The compiler was multi-pass and included all modern code-improvement methods in addition to some developed internally.

Software Engineer, Horizon Research Laboratories, Fort Collins, CO. 1/87 – 9/87. Part of a three-person team which produced C compilers for different wide-word graphics processors. Created or helped with the creation of many of the analysis and code-improvement routines that were written in C. These included cover analysis, memory reference disambiguation, intermediate optimizations, graph-coloring register assignment, code selection, software pipelining and trace scheduling, and a peephole optimizer.

AFFILIATIONS:

Association for Computing Machinery

IEEE

North Texas Net-Centric Software and Systems Consortium

Teach North Texas

Computer Science Teachers Association

RESEARCH COLLABORATORS:

Steve Carr, Michigan Technological University
Krishna Kavi, University of North Texas
Hao Li, University of North Texas
Cameron Palmer, University of North Texas
Patrick Burke, University of North Texas
Steve Beaty, Metrostate Denver
Vicki Allan, Utah State University
Bo Gong Su, Patterson College

CURRENT PHD STUDENTS:

Cameron Palmer
Patrick Burke

ALUMNI:

Michael J. Bourke, III. Frequency-Based Scheduling: An Extension of List Scheduling to Incorporate Frequency Information. (Masters)
Thomas Brasier, FRIGG: A New Approach to Combining Register Assignment and Instruction Scheduling. (Masters)
Chen Ding, Improving Software Pipelining with Unroll-and-Jam and Memory Reuse Analysis. (Masters)
Jason Hiser, Register Bank Assignment for Partitioned Register File Machines. (Masters)
Brett Huber, Path-Selection Heuristics for Dominator-Path Scheduling. (Masters)
Saurabh Jang, Generating Efficient Code for VLIW Architectures with Partitioned Register Files. (Masters)
Darla Kuras, Using Value Cloning to Improve Code Generation for Software Pipelined Loops on VLIW Architectures with Partitioned Register Files (Masters)
Yi Qian, Loop Transformation for Clustered VLIW Architecture.
M. Premanand Rao, Combining Register Assignment and Instruction Scheduling. (Masters)
Evan Schemm, Using FIFO Replacement to improve Icache Hit Rates. (Masters)
Evan Schemm Icache Hit Rates in ILP Architectures (Dissertation). Associate Professor, Computer Science, Lake Superior State University, Sault Ste. Marie, MI.
Tom Suchyta, Global Reduction of Spill Code by Live-Range Splitting. (Masters)
Dineel Sule, An Evaluation of Existing Heuristics for Register Bank Partitioning Using Genetic Algorithms. (Masters)
Craig Webb, CISC Instruction Identification Using Data Dependence Graphs. (Masters)
Chris Wolf, I2R: Combining Source-Level Analysis with Code Generation for ILP Architectures. (Masters)
Qunyan WU, Register Allocation via Hierarchical Graph Coloring (Masters)

UNDERGRADUATE RESEARCHERS:

Scott Colcord, Instruction Scheduling with Genetic Algorithms, Summer and Fall, 1995;

Pete Curry, Evaluation of Scale code generation, Summer 2006

Dan Daugherty, Developing Compiler tools for use in an undergraduate course, Spring and Fall 2006

Jack Lindamood, Porting an existing compiler a new Linux environment, Spring 2006

Jeremy Wilson, Experimental Evaluation of Compiler Phase Order on Code Generation, Spring and Fall 2005

PROFESSIONAL SERVICE:

- Program committee member for ESO 2008 (3rd International Workshop on Embedded Software Optimization), to be held in Shanghai, China in December 2008.
- Program committee member for HASE 07 (10th IEEE International Symposium on High Assurance Systems Engineering), to be held in Dallas in November 2007.
- Program committee member for SCOPEs 07 (Software and Compilers for Embedded Systems), held in Nice, France in April 2007
- Program co-chair of SCOPEs 05 (Software and Compilers for Embedded Systems), held in Dallas in September 2005
- Program committee member for ACM International Conference on Computing Frontiers, held in Ischia, Italy in May 2005
- Program committee member for LCTES 2003 (Languages, Compilers and Tools for Embedded Systems), held in San Diego in June 2003
- Program committee member for MICRO 1995.
- Reviewer for many conferences and journals over the last 20 years.

UNIVERSITY SERVICE:

- Chair, College Tenure and Promotion Committee, 1998-2000
- Director of Graduate Studies, CS department, 1992-94, 1999-2000
- CS department representative to University Senate 1995-98.
- Member of several CS department committees, including undergraduate curriculum, equipment, graduate, space, faculty search.
- Member of university search committee for Vice-Provost for Instruction
- Member of University Senate Research Policy committee
- Co-author of and instructor in MTU's "Orientation for New Faculty", 1995-96. For the first time, new faculty orientation focused on teaching. This included an intensive two-day workshop and weekly seminars throughout the year.
- Chair, Faculty Search committee (2003-2004)
- Member, Executive committee (2003-2005, 2007-2009)
- Member, Research Enhancement Committee (2004-2005)
- Member, ad hoc Computer Engineering steering (2003-2004)
- Member, Graduate Studies Committee (2005-2008)
- Member, Undergraduate Committee (2005-2006, 2008-2009)
- Supervision of 9 TAs, and 7 RAs.